

1                   **ABSTRACT OF THE DISCLOSURE**  
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3                   An integrated circuit includes a heterojunction thyristor device having an anode  
4                   terminal, a cathode terminal, a first injector terminal operably coupled to a first quantum  
5                   well channel disposed between the anode terminal and the cathode terminal, and a second  
6                   injector terminal operably coupled to a second quantum well channel disposed between  
7                   the anode terminal and the cathode terminal. Bias elements operate the heterojunction  
8                   thyristor device in a mode that provides substantially linear voltage gain for electrical  
9                   signals supplied to at least one of the first and second injector terminals for output to at  
10                  least one output node. Preferably, the bias elements include a first DC current source  
11                  operably coupled to an n-type modulation doped quantum well structure, a second DC  
12                  current source operably coupled to a p-type modulation doped quantum well structure, a  
13                  first bias resistance operably coupled between a high voltage supply and the anode  
14                  terminal, and a second bias resistance operably coupled between the cathode terminal and  
15                  a low voltage supply. The bias elements provide a current passing from the anode  
16                  terminal to the cathode terminal that is below a characteristic hold current for the  
17                  heterojunction thyristor device to thereby inhibit switching of the heterojunction thyristor  
18                  device. The DC current provided by the DC current sources controls the amount of  
19                  voltage gain provided by the heterojunction thyristor device.